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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/458,551	12/09/1999	ALEXANDER JOFFE	M-5648-ID-US	8981

32605 7590 06/18/2004

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EXAMINER	
BANANKHAH, MAJID A	

ART UNIT	PAPER NUMBER
2127	

DATE MAILED: 06/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/458,551	JOFFE ET AL.	
	Examiner	Art Unit	
	Majid A Banankhah	2127	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14,15 and 17-68* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14,15 and 17-68* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/05/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. This final office action is in response to the amendment and remarks filed on April 19, 2004. Applicant's arguments with respect to claims 14-29 have been fully considered but they not deemed to be persuasive. In view of applicant's amendment, the rejection of claims under 112 second paragraph in the previous office action dated February 26, 2004 is hereby withdrawn. Applicant's amendment necessitated the new ground of rejection. Claims 14-15, and 17-68 are considered for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 14-15, 18, 23-24, 30-33, and 50-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okin (U.S.Pat. No. 5,361,337, hereinafter Okin) and Uchiyama et al. (U.S.Pat., No. 4,797,816, hereinafter Uchiyama).

Per claims 14, 18 and 23, the reference of Okin teaches of:

a processor for executing instructions such that when the processor executes a first instruction and the processor determines after starting to execute the first instruction that the first instruction is blocked (col. 2, lines 29-36, Having multiple copies of state elements on the processor and coupling them to a multiplexer permits the processor **to save the context of the current instructions** and **resume executing new instructions within one clock cycle**).

The reference of Okin does not explicitly teach whether he resume the execution from the point where he suspended the instruction (because of cache miss or any other hazard condition)

or re-execute the instruction from the start of the instruction. However, Uchiyama teach of a problem associated with starting the execution when a fault condition (such as cache miss, page fault or a hazard or resource is unavailable) occurs and how it is advantageous to re-execute the instruction (or restart from the beginning of the instruction) after the fault condition is over (exception handler solve the cache miss or page fault or resource becomes available). See Uchiyama, col. 1, lines 26-34, lines 45-52, line 58 to line3 in col. 2. Therefore, it would have been obvious for one ordinary skill in the art at the time the invention was made to re-execute the instruction after an instruction is blocked for the reason that the overhead associated with saving and restoring the context is eliminated (See, Uchiyama, col. 1, lines 58-61, and col. 3, lines 36-43).

Regarding the limitation of aborting the execution of the first instruction, the reference of Uchiyama teaches of recovering only the value of registers necessary for calculation of the effective address of an operand which inherently teaches that the instruction is aborted after it encountered a fault (Uchiyama, col. 36-43, In the re-execution of instructions, the present invention provides that only the values of registers necessary for calculation of the effective address of an operand are recovered), for the reason to free up memory space and increase efficiency.

Regarding the multitasking limitation in claim 18, see Okin col. 1, lines 62-68.

Per claim 30, and 50, the processor of Claim 14 wherein:

the processor comprises an instruction execution unit for executing instructions stored in a memory and fetched from the memory; the processor aborts the first instruction after the first instruction has been fetched from the memory; and the processor again fetches the first instruction from the memory to re-execute the first instruction. The details of storing instruction

and recovery into and from the memory for re-execution is taught by Uchiyama in col. 2, line 60 to col. 3, line 35.

Per claims 31 and 51, the processor of Claims 14/23 wherein the first instruction is aborted after being decoded by the processor, and the first instruction is decoded again when the first instruction is being re-executed by the processor. See Uchiyama for decoding instruction every time the instruction is aborted and/or re-executed (col. 4, lines 16-30, and lines 41-49).

Per claims 32 and 52, the processor of Claims 14/23 wherein the first instruction is blocked if the first instruction is to access a resource unavailable for the first instruction. The blocking of instruction is well known in the art and it is suggested by Okin and Uchiyama (claim 1, and col. 4, lines 41-49 respectively).

Per claims 33 and 53, the processor of Claims 32/52 wherein the resource is a storage area. Okin teaches of cache miss and Uchiyama teaches of Page fault (Abstract, and col. 2, lines 3-11 respectively).

Per claims 15 and 24, the processor claims 32/52 wherein the processor re-executes the first instruction when the resource becomes available. The system of Uchiyama teaches of the limitation in col. 1, lines 26-34, lines 45-52, line 58 to line3 in col. 2.

4. Claims 34-36 and 54-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okin (U.S.Pat. No. 5,361,337, hereinafter Okin) and Uchiyama et al. (U.S.Pat., No. 4,797,816, hereinafter Uchiyama) and Hendel et al. (U.S.Pat., No. 5,175,732, hereinafter Hendel).

Per claims 34-36, and 54-56, Okin disclose a system for switching the context of state elements of a very fast processor within a clock cycle. The processor disclosed does not know what kind or instruction it is processing, therefore, it is obvious to use Okin's processor for any environment including network data for the reason to minimize the average instruction cycle time for the processor with a main memory access time exceeding processor clock cycle. The system of Hendel discloses a networking environment wherein the command and status interface unit further comprises command routing means for selectively routing the receive commands to the first FIFO storage unit, the transmit commands to the second FIFO storage unit, miscellaneous commands to the medium access control unit, and clearing commands to the third and fourth FIFO storage units. Later he teaches of request FIFO, command FIFO, and status FIFO in col. 10, lines 55, line 55 to col. 11, line 7. Therefore, it would have been obvious for one ordinary skill in the art at the time the invention was made to use Okin's modified processor in the networking environment of Hendel, for the reason to minimize the average instruction cycle time for the processor with a main memory access time.

5. Claims 17, 19-22, 25, 26-29, 37-39, 40, 57-59, and 60-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okin (U.S.Pat, No. 5,361,337, hereinafter Okin) and Uchiyama et al. (U.S.Pat, No. 4,797,816, hereinafter Uchiyama), and Hendel et al. (U.S.Pat, No. 5,175,732, hereinafter Hendel), and Nemirovsky (DYNAMIC INSTRUCTION STREAM COMPUTER, Apple Computer Corporation, 1991, Dr. Mario Daniel Nemirovsky).

Per claims 37and 57, the processor of Claim 17 wherein when the first instruction is aborted, the processor is operable to suspend the first task and to execute another task instead of the first task while the first task is suspended. The system of Okin fails to explicitly teach of the limitation,

However, Nemirovsky, teaches of dynamic interleaving in a pipeline processing environment wherein a task can be executed when a first task is suspended (See page 166, under dynamic interleaving, even when interrupts are invoked, other task can be running). Therefore, it would have been obvious for a person ordinary skill in the art at the time the invention was made to use Nemirovsky's interleaving method in Okin's processor because it will eliminate the overhead of context switching and by doing that efficiency will be increased.

Per claim 38, and 58, the processor of Claim 37 wherein suspension of the first task and scheduling of the other task instead of the first task does not involve instruction execution by the processor. The method of Nemirovsky does not require instruction execution.

Per claim 39, and 59, the processor of Claim 37 wherein the first task remains suspended at least until the resource becomes available to the first task. Uchiyama teaches that: "In case of a page fault, it is necessary to restore the contents of registers to re-execute the instructions. Such cases are for example as in the following" (col. 2, lines 60 to col. 3, line5). This implies that until the register content is not recovered, the task remains suspended.

Per claims 17, the processor of Claim of claim 32 wherein the processor performs multi-tasking, and the resource is unavailable for the first instruction if the resource is unavailable to a first task executing the first instruction. Okin teaches of multitasking environment and cache miss in col. 1, lines 62-68.

Per claim 25, the method of Claim 52 wherein executing the first instruction comprises executing the first instruction by a first task, and the resource is unavailable to the first task. Uchiyama teaches of the limitation in col. 1, lines 58- to col. 2, line 2.

Per claims 19 and 26, see the rejection of claim 14 above.

Per claims 20 and 27 see Okin, col. 3, lines 28-44, and the rejection of claim 39 above.

Per claims 21 and 28, see Okin, col. 3, lines 45-61.

Per claims 22 and 29, see Okin, col. 4, lines 1-26.

Per claim 40, the system of Okin teaches of interleaving of the task sin a pipeline processing environment (see, Nemirovsky, page 165, R.col. section 3.4). In there tasks from different group can be interleaved. Therefore, when the first instruction from the first task is suspended, another task from another group is executed.

Per claims 41 and 60, see the pipeline interleaving section in Nemirovski (See page 166, under dynamic interleaving, even when interrupts are invoked, other task can be running).

Per claims 42 and 61, see re-execution of instructions of the first task after the fault condition is over (exception handler solve the cache miss or page fault or resource becomes available, See Uchiyama, col. 1, lines 26-34; lines 45-52, line 58 to line3 in col. 2).

Per claims 43 and 62, see Uchiyama for decoding instruction every time the instruction is aborted and/or re-executed (col. 4, lines 16-30, and lines 41-49).

Per claims 44 and 63, see Uchiyama, col. 4, lines 15-30 (if the content of a register is altered by storing therein a word read out based on the effective address obtained through addition of a displacement to the content of the register in execution of one instruction, the name of the altered register and the value of the displacement used for alteration are tagged and saved in a specified control register).

Per claims 45 and 64, interleaving is a way to share processor resources between multiple processes (see Nemirovsky, page 165, left col. Section 3.3).

Per claims 46 and 65, see Nemirovsky, page 165, Interleaving, he teaches of shared resources including storage area.

Per claims 47-49, and 66-68, please see the rejection of claims 34-36 section 4 above.

6. Applicant on page 16 of his remarks argue in substance that "Okin does not teach or suggest that the processor later re-executes the current instruction and not simply resumes the current instruction) when the data me brought into the cache. Therefore, Okin does not teach or suggest Applicants invention". In response, applicant's attention is respectfully directed to the rejection of claims in this office action (section 3 above) and the teaching of Uchiyama in col. 1, lines 26-34, lines 45-52, line 58 to line3 in col. 2. In there he teaches of a problem associated with starting the execution when a fault condition (such as cache miss, page fault or a hazard or resource is unavailable) occurs and how it is advantageous to re-execute the instruction (or

restart from the beginning of the instruction) after the fault condition is over (exception handler solve the cache miss or page fault or resource becomes available).

Later on page 17, applicant argues: "Okin does not teach or suggest fetching the instruction again on a cache miss. To the extent that Okin's duplication of the state elements may avoid the need to re-fetch the Okin does not teach or suggest decoding the instruction again on a cache miss. To the extent that Okin's duplication of the state elements may avoid the need to re-decode the instruction, Okin teaches away from the invention of Claim 31." In response, please see the teaching of Uchiyama in col. 4, lines 16-30, and lines 41-49, for decoding instruction every time the instruction is aborted and/or re-executed.

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8. **Applicants amendment necessitated the new ground of rejection. THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. § 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. § 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE The application has been amended as follows:
ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Maid A. Banankhah** whose voice telephone number is **(703) 308-6903**. A voice mail service is also available at this number.

All response sent to U.S. Mail should be mailed to:

Commissioner of Patent and Trademarks

Washington, D.C. 20231

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is **(703) 305-9600**.

Maid Banankhah

6/16/04

MAJID BANANKHAH
PRIMARY EXAMINER